WIDE ADDER WITH CRITICAL PATH OF THREE GATES

ABSTRACT OF THE DISCLOSURE

Apparatus and method for performing fast arithmetic operations, including addition, in a pipelined circuit. In one embodiment, the apparatus comprises a plurality of gates, the critical path through the plurality of gates being three gates delays for some embodiments. The apparatus may comprise: a first level of logic for receiving at least two binary numbers and generating multi-bit P, G, Z, and K carry signals; a second level of logic receiving the multi-bit P, G, Z, and K carry signals and generating multi-bit section-based carry signals; and a third level of logic receiving the multi-bit section-based carry signals and generating a sum of the received binary numbers, the third level of logic comprising: a plurality of domino logic gates forming sum bits using the multi-bit section-based P, G, Z, and K carry signals.